**Q.P. Code: 16EC402** **R16**

**Reg. No:** | | | | | | | | | | |

**SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR**

(AUTONOMOUS)

**B.Tech II Year I Semester Supplementary Examinations July - 2022**

**SWITCHING THEORY & LOGIC DESIGN**

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

**UNIT-I**

**1** Convert the given decimal number 234 to binary, quaternary, octal, hexadecimal and BCD equivalent. **12M**

**OR**

**2** **a** State Duality theorem. List Boolean laws and their Duals **6M**

**b** Simplify the following Boolean functions to minimum number of literals: **6M**

i. F = ABC + ABC' + A'B ii. F = (A+B)' (A'+B')

**UNIT-II**

**3** **a** Simplify the following Boolean expressions using K-map **6M**

F(W,X,Y,Z)= XZ+W'XY'+WXY+W'YZ+WY'Z

**b** Implement the same using NAND gates. **6M**

Simplifying the following expression using tabulation technique.

**OR**

**4** Simplify the following Boolean function in POS form using K-map **12M**

F(A,B,C,D) = Σ(1,2,4,5,9,12,13,14)

**UNIT-III**

**5** **a** Design & implement Full Adder with truth table. **6M**

**b** Design & implement Full Subtractor with truth table. **6M**

**OR**

**6** Implement 4-bit Magnitude Comparator and write down its design procedure. **12M**

**UNIT-IV**

**7** **a** Draw the logic symbol, characteristics table and derive characteristics equation of JK flip flop. **6M**

**b** Design T Flip Flop by using JK Flip Flop and draw the timing diagram. **6M**

**OR**

**8** With a neat sketch explain MOD 6 Johnson counter using DFF. **12M**

**UNIT-V**

**9** Implement the following Boolean function usingPLA **12M**

(i)F1= Σm(0,1,2,3,8,10,12,14)

(ii)F2 = Σm(0,1,2,3,4,6,8,10,12,14).

**OR**

**10** Discuss Mealy & Moore Machine models of sequential machines. **12M**

*** END ***